Trials and Tribulations of Early PCIe® 4.0 Adoption

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Agenda

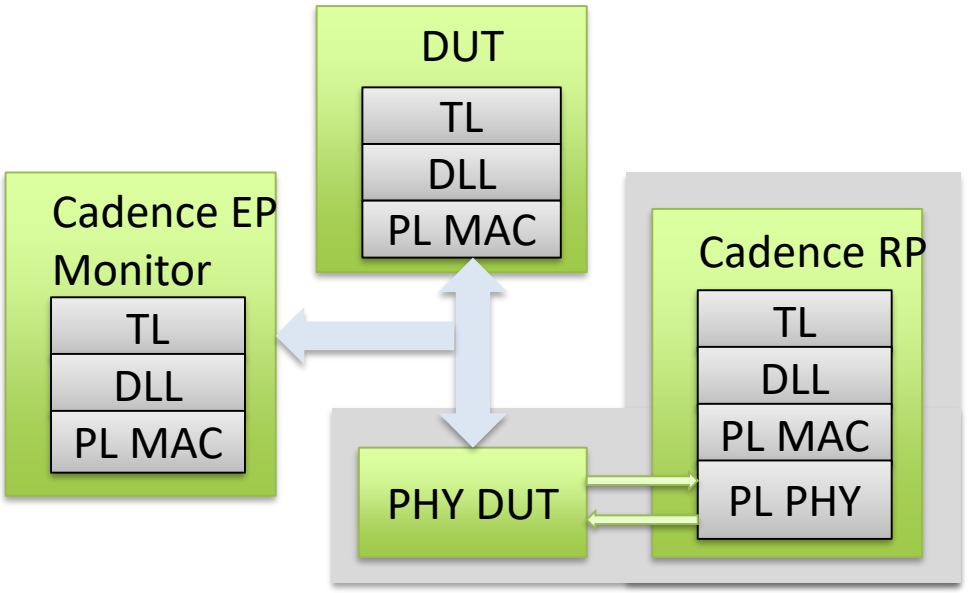
- **Verification Challenges of PCIe® 4.0**
- **Overview of PCIe 4.0 Verification Environment**
- **PCIe 4.0 New Feature Verification**
  - Scaled Flow Control
  - Fault Isolation
  - Equalization
- **Lesson Learned**
- **Conclusion**

Verification Challenges of PCIe 4.0

- **Time to market**
- **Tracking changes to PCIe 4.0 Base Specification**
- **Guarantee the Quality of IP**
- **Compliance testing**

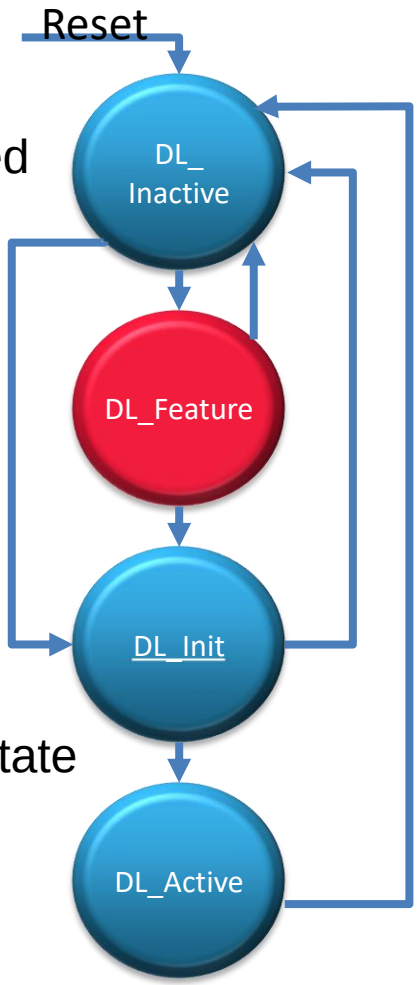
Verification Environment

- **Vera based random verification**
- **Leverage Cadence PCIe VIP to generate the stimulus and monitor DUT behavior**
- **DUT is a Endpoint supporting 4.0 speed with PIPE Interface**



Scaled Flow Control

- **Problem**
  - Although bandwidth is higher, latency is mostly unchanged
  - Results in platforms running into limits for flow control
  - Flow control credits is independent of link speed
- **Goal**
  - Maintain backward compatibility
  - Scale flow control credits with link speed
- **Verification Challenges**
  - Ensure previous generations function correctly
  - Verifying new Data Link Feature DLLP and DL_Feature state
  - Exhaustive testing of HdrScale and DataScale



Scaled Flow Control Verification

- **DUT**
  - Only support HdrScale and DataScale as 00/01 locally
  - Support all possible Scaled Value from remote side
- **How to Verify**
  - Randomly set local Scaled Flow Control support and Data Link Feature Exchange Enable in both DUT/Cadence Denali RP before simulation.
  - Randomly set HdrScale and DataScale for P/NP/CPLD in Cadence Denali RP side and collect coverage in Cadence Denali monitor call back

Fault Isolation Verification

- **DUT**
  - Fully support this feature
- **Verification Challenges**
  - Not easy to develop SKP_END_CTL Parity Algorithm model
- **Goal**
  - SKP_END_CTL Algorithm/transmit rule
  - 16GT/s Local Data Parity Mismatch Status Register
- **How to Verify**
  - Cadence Denali monitor check algorithm & transmit rule
  - Inject error on Cadence Denali RP callback when transmitting SKP_ENC_CTL and check in DUT CFG

Equalization

- **Problem**
  - Inter symbol interference (ISI) – distortion of a signal in which one symbol interferes with subsequence symbols is a bigger problem with higher PCIe 4.0 speeds
- **Goal**
  - More “reactive” adaption of signal versus setting constant de-emphasis as was the case for PCIe 1.0 and PCIe 2.0
  - Error injected scenario
- **Verification Challenges**
  - Ensure LTSSM modeling is correct otherwise training to PCIe 3.0 and beyond is not possible
  - Exercise multiple protocol registers correctly (registers exists per lane)
  - May timeouts and rules related to the process

PCIe 4.0 Equalization Verification

- **DUT**
  - Fully support this feature
- **Scenarios to be tested**
  - Normal EQ Progress will be checked by Cadence Denali Monitor
  - EQ Bypass Scenario(phase may be skipped)
  - EP Timeout Scenario(In which timeout when adjusting EQ coefficient)
  - Equalization Redo Scenario

Compliance Test

- **Verification Challenges**
  - We may get different understanding on the base spec, especially the updated part.
  - Bugs are hard to be found if test bench writer make same mistake as designer
- **How**
  - Use VIP monitor to monitor DUT's behavior through PIPE interface
  - For Capabilities:
    - ✓ Issue random CFG read from RP, monitor will check the returned data
    - ✓ go-through all the CFG capabilities for some special scenario like link disable, hot reset and FLR

Lesson Learn 1#

- **Performance Test should be scheduled in early state**
  - As PCIe 4.0 PIPE CLK will run on 1GHz, Performance may be impacted when fix some timing issue
  - Ideal transfer speed for outbound write at PCIe 4.0 speeds is 32GB/s. However, initial RTL performance was 26.86GB/s and after fixes we were able to achieve 30.36GB/s

Lesson Learn 2#

- **An Interesting Scenario related to Scaled Tag**
  - DUT ONLY support 10-bit tag feature as **completer**
  - Think about below Scenario:
  - Some explanations:
    1. The DUT is not capable of generating a 10-bit Tag, so it should act as if it is an 8-bit Tag generator. Before 10-bit Tags were defined, the bits that are now Tag[9:8] were Reserved, and receivers are explicitly requires to ignore Reserved bits.
    2. In general, the DUT "understands" 10-bit Tags. It knows that it didn't generate a Tag with Tag[9:8] != 00, so it could declare that there is a mismatch and it has received an Unexpected Completion.

  Option 1 is adopted

1. DUT send MRd (tag = 0x02)
2. Cadence Denali RP return a completion with tag = 0x102 (all other attribute in completion is correct, this completion is generated on purpose)
3. DUT accepts this completion, and sends another memory read with tag = 0x02

?? Is it correct?

Lesson Learn 3#

- **Related to the Minimum initial Flow control Advertisements**
  - Take PD for example
  - explain the +1 here:

Ceiling(Largest Max_Payload_Size / (FC Unit Size * 16)) + 1. For a Multi-Function Device, this includes all Functions in the device.

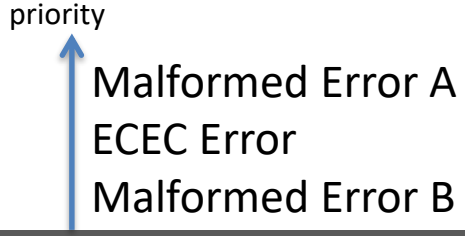
Example: If the largest Max_Payload_Size value supported is 1024 bytes, the smallest permitted initial credit value would be 005h.

  - Test Scenario:

- DUT act as EP, support PCIe 4.0, MayPayload size(MPS) = 4096
- Denali VIP act as RP, support PCIe 4.0 with Scaled Factor = 16 (x16),MPS= 4096, PD credit allocated = 16 (while the min value in base spec is 4096/256+1=17)
- DUT firstly send a mem write to RP with 1 DW payload
- RP will not update credit after receive this TLP, as data credit factor is x16
- DUT wants to send a 4096 TLP, however, DUT finds that credits are not enough. Thus hung

Lesson Learn 4#

- **Some thinking on Error Pollution**
  - PCIe 3.0 and 4.0 get different priority for *Malformed TLP* and *ECRC Check Failed* (in 4.0, Malformed TLP get higher priority)
- **DUT deal with it with a different way**
  - DUT handles related TLP like this:
  - Malformed Error A
    - Although this TLP pass LCRC check, but it seems that it is not trustable (header size not match Fmt, payload size larger than MSP, data specified by length not match actual data…)
    - This TLP shouldn't have been received at all (Assert_INTx Message is received by EP, A Msg/MsgD Request specifies 000b routing at the Upstream Port of a Switch.)
  - ECRC ERROR
  - Malformed Error B(Address/length combination crosses a 4 KB address boundary, BE violation…)



Conclusion

- **Using Verification IP can largely ease the PCIe 4.0 verification work**
- **Random based simulation help to hit corner case**
- **Verification challenge for next PCIe generation**
  - Faster speed make it harder to understand/verify physical layer related logic
  - IP architecture may be impacted by faster speed
  - Backward compatibility test

Acknowledgement

- **PCI-SIG®**
- **Fei Cao**
- **XingGuang Pan**
- **Paul Mattos**
- **Peter Jenkins**

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